#25873

MJ1602

ORIGINAL

WESTERN DIGITAL
CORPORATION

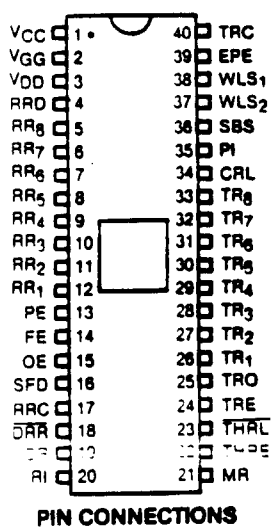
TR1402/TR1602
Universal Asynchronous Receiver/Transmitter (UART)

FEATURES

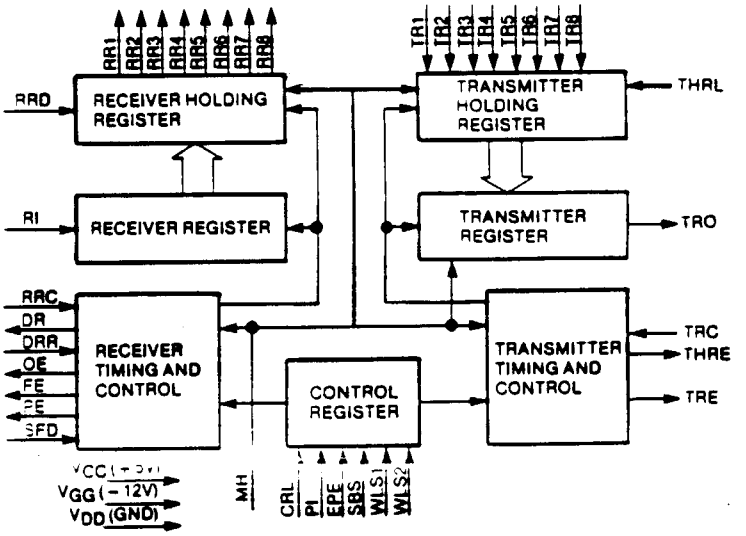
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  - Word Length
  - Baud Rate
  - Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
    - Parity Inhibit
  - One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level for TR1602)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  - Transmission Complete
  - Buffer Register Transfer Complete
  - Received Data Available
  - Parity Error
  - Framing Error
  - Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  - Receiver Register Outputs
  - Status Flags
- TTL COMPATIBLE
- PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES



PIN CONNECTIONS



TR1602/TR1402 BLOCK DIAGRAM

GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UART) is a general purpose, programmable or hardwired MOS/LSI device. The UART is used to convert parallel data to a serial data format on the transmit side, and converts a serial data format to parallel data on the receive side.

The serial format in order of transmission and reception is a start bit, followed by five to eight data bits, a parity bit (if selected) and one, one and one-half (1602 bit data format only) or two stop bits.

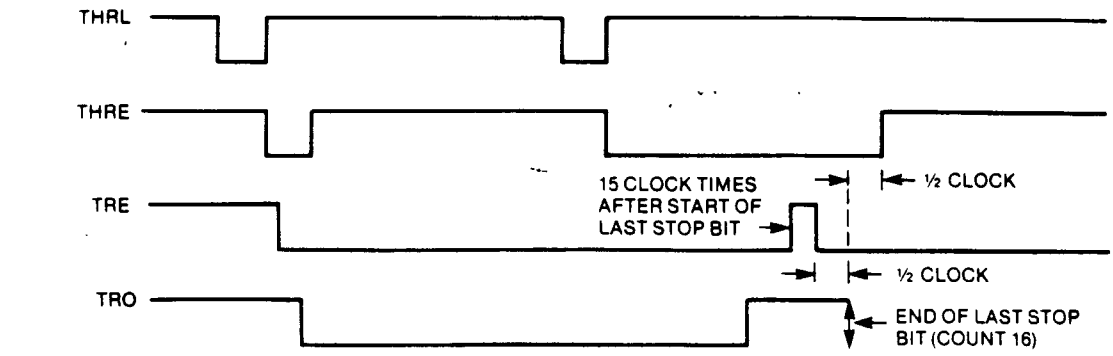
Three types of error conditions are available on each received character: parity error, framing error (no valid stop bit) and overrun error.

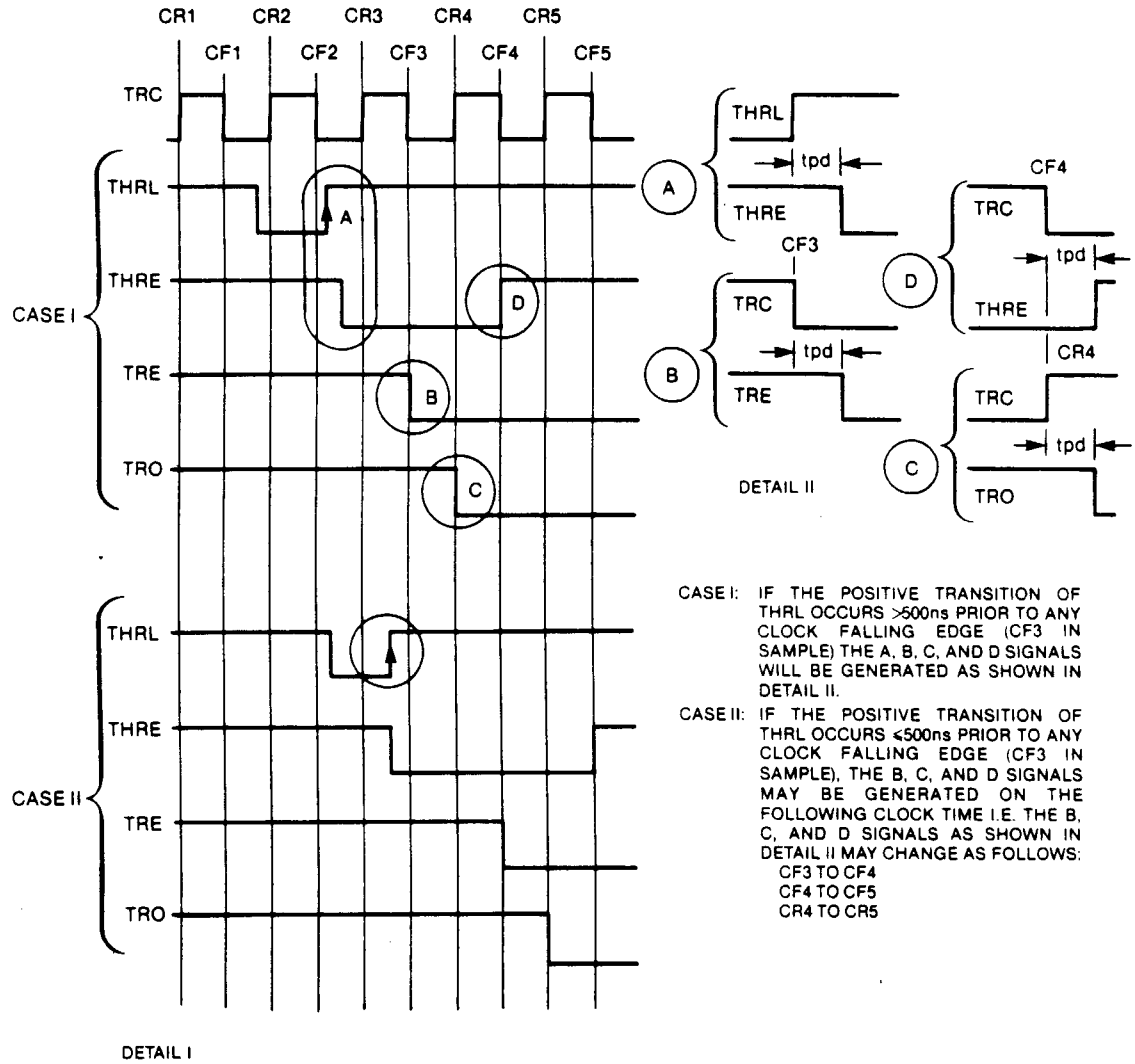
The transmitter and receiver operate on external 16X clocks, where 16 clock times are equal to one bit time. The receiver clock is also used to sample in the center of the serial data bits to allow for line distortion.

Both transmitter and receiver are double buffered allowing a one character time maximum between a data read or write. Independent handshake lines for receiver and transmitter are also included. All inputs and outputs are TTL compatible with three-state outputs available on the receiver, and error flags for bussing multiple devices.

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	VSS	+5 volts supply
2	POWER SUPPLY	V_{GG}	-12 volts supply
3	POWER SUPPLY	V_{DD}	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_{1-8} data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PARITY ERROR	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity differ from that which is programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).





CASE I: IF THE POSITIVE TRANSITION OF THRL OCCURS >500ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE) THE A, B, C, AND D SIGNALS WILL BE GENERATED AS SHOWN IN DETAIL II.

CASE II: IF THE POSITIVE TRANSITION OF THRL OCCURS ≤500ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE), THE B, C, AND D SIGNALS MAY BE GENERATED ON THE FOLLOWING CLOCK TIME I.E. THE B, C, AND D SIGNALS AS SHOWN IN DETAIL II MAY CHANGE AS FOLLOWS:
- CF3 TO CF4
- CF4 TO CF5
- CR4 TO CR5

TRANSMITTER TIMING